

Contact ↓ +44 (1295) 201250 M info@firsteda.com www.firsteda.com

FirstEDA specialises in the distribution and support of leading-edge EDA solutions for European electronics designers involved in the specification, implementation, verification and certification of custom silicon devices.







Aldec delivers innovative design creation, simulation and verification solutions to assist in the development of complex FPGA, ASIC, SoC and embedded system designs. FirstEDA is proud to be the sole distribution and support channel for Aldec in the UK, Ireland, Netherlands, Nordic countries, France, Spain, Belgium and Portugal.

Active-HDL FPGA Design & Simulation; **ALINT-PRO** Advanced Design Rule Checking; **Riviera-PRO** Advanced Verification Platform; **TySOM EDK** High performance Embedded Development kits; **DO-254 CTS** FPGA Level In-Target Testing; **HES-7** ASIC Prototyping; **HES-DVM** Hardware Assisted Verification; **RTAX/RTSX** Prototyping Microsemi Rad-Tolerant Devices

Agnisys is a leading supplier of EDA software for solving complex design and verification problems for system development. Their products provide a common specification-driven development flow to describe registers and sequences for system-on-chip (SoC) and intellectual property (IP). Enabling faster design, verification, firmware, and validation.



IDesignSpec Design and Verification of SoC addressable registers; **IDS-Verify** Test and testbench specification automation; **IDS-Validate** Automated pre-silicon and post-silicon validation; **IDS-Integrate** Automated Chip Assembly from Specification; **IDS-IPGen** Specification automation for standard and custom IP blocks

Sigasi;

Sigasi delivers solutions that help HDL design engineers deliver validated designs faster and more efficiently. The Sigasi Studio development platform is the compelling next-generation IDE for VHDL, Verilog and SystemVerilog and is being used by some of the biggest names in aerospace, defence, consumer electronics, industrial automation, medical electronics and telecom.

Sigasi Studio XL Design Entry, Browsing and Advanced Linting; **Sigasi Studio XPRT** Design Entry, Browsing, Advanced Linting, Interactive Diagrams and Documentation; **Sigasi Veresta** Code checks in your CI/CD flow

Language and Methodology Training - Classroom or online, live and interactive



FirstEDA offers internally developed, high quality instructor-led training in tool proficiency and languages & methodologies, as well as training developed and delivered through our partnership with US-based VHDL specialists SynthWorks. FirstEDA's own engineering experiences add great value and ensure the training is fit-for-purpose and current.



Our training courses are engaging, practical and sociable, and we certainly haven't lost sight of the fact that engineering is both interesting and rewarding. Whether attending to learn new skills or to enhance your current ones, you will be mixing with like-minded individuals, all of whom are keen to learn new techniques and methodologies that will further their careers.

VHDL for FPGA Designers *Instructor-led, live and interactive (2 days classroom or 3 days online)*

Our two (2) day instructor led VHDL language and application training provides a thorough background in the use and application of synthesisable VHDL in digital hardware design. The training is structured around a set of basic component building blocks and uses these devices to demonstrate the application of the VHDL language.

Intermediate VHDL Instructor-led, live and interactive (3 days classroom or 5 days online)

Ready for the next step? For those already familiar with VHDL (either through an introductory course or self-taught), this workshop will broaden knowledge and enforce competency through application. Specifically constructed to bridge the gap between basic working knowledge of VHDL and our Advanced VHDL Testbenches & Verification course.

Advanced VHDL Testbenches & Verification Instructor-led, live and interactive (delivered by Jim Lewis of SynthWorks) (5 days classroom or 10 days online)

Our Advanced VHDL training course teaches the latest VHDL Verification techniques and methodologies for FPGAs and ASICs, including the Open Source VHDL Verification Methodology (OSVVM). Our methodology works with any simulator that supports VHDL-2008, removing the requirement to learn a new language or invest in new and costly tools.

Part 1: Essential VHDL Verification (3 days classroom or 6 days online)

You will learn to create structured transaction-based testbenches using either procedures or models (aka: verification IP or transaction level models). Both of these methods facilitate creation of simple, powerful, and readable tests.

Part 2: Expert VHDL Verification (2 days classroom or 4 days online)

Building on the core topics covered in Essential VHDL Verification, Expert VHDL Verification teaches advanced topics including modeling multi-threaded models (such as AXI4-Lite), advanced functional coverage, advanced randomisation, creating data structures using protected types and access types, timing and execution, configurations and modeling RAM.



About FirstEDA

Established in 2002, FirstEDA is a highly responsive value-added distributor of EDA tools and training in Europe.

The company comprises a team of highly skilled engineers and it is the trusted sales partner-of-choice for a number of EDA vendors; each of which has a range of innovative and versatile products.

As experienced engineers, FirstEDA ensures the solutions it promotes and supports are fit-for-purpose and that they are able to tackle today's most demanding challenges. Moreover, the company works extremely closely with the vendors' product specialists so, on the rare occasions when additional support is needed, FirstEDA provide a fast turnaround.

FirstEDA Limited Castle Hill House, 12 Castle Hill Windsor, SL4 1PD, UK ↓ +44 (1295) 201250 ⊠ info@firsteda.com □ www.firsteda.com

Copyright © 2023 FirstEDA Limited. All rights reserved. All brands or products are the trademarks or registered trademarks of their owners.







