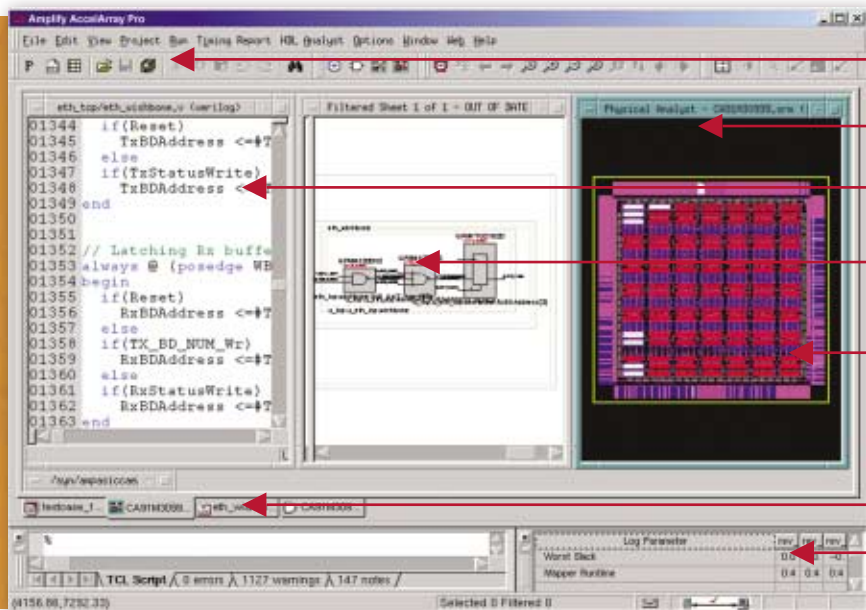


Amplify[®] AccelArray[™] Pro

STRUCTURED/
PLATFORM ASIC
DATASHEET

Enhanced Physical Synthesis Tool

Exceptional Performance and Density for Fujitsu's AccelArray Structured ASICs



The screenshot displays the Amplify AccelArray Pro software interface. It features a menu bar at the top with options like File, Edit, View, Project, Run, Timing Report, HDL, Physical, Options, Window, Help, and Exit. Below the menu bar is a toolbar with various icons. The main workspace is divided into several panes: a code editor on the left showing Verilog code, a 'Filtered Sheet 1 of 1 - OUT OF DATE' pane in the center, and a 'Physical Analyst - CASH0000_0000_0000' pane on the right showing a grid-based floorplan. A 'Log Parameter' window at the bottom right shows timing data. Red arrows point from text labels on the right to specific features in the software interface.

- Integrated, ultra-fast static timing analysis
- Legal placement of your design
- Custom optimization for AccelArray architecture
- Integrated Physical Analyst[™] feature for enhanced visualization and debugging
- Automatic and manual floorplanning
- TCL command line interface
- Watch window for easy review of results for multiple implementations

The only Fujitsu-certified physical synthesis solution for AccelArray designs

The Amplify AccelArray Pro physical synthesis solution provides a single integrated design environment from which the AccelArray designer can: create and edit floorplans; perform AccelArray-specific physical synthesis; interactively analyze and modify the design specification; and, complete a legally placed gates design ready for handoff to Fujitsu. This solution is the result of a joint development between Synplicity and Fujitsu, and is fully integrated with Fujitsu AccelBuilder tools.

Highest quality of results and predictability

AccelArray frames have a very specific architecture that requires custom physical optimizations if your design is to meet timing in the smallest possible area. The Amplify AccelArray Pro solution uses its unique knowledge of the AccelArray architecture and design rules to perform custom physical synthesis that dramatically improves quality of results (QoR). Techniques include:

- Direct mapping to create area efficient results.
- Custom mapping to dedicated AccelArray frame resources.

- Custom module generators that implement arithmetic modules in the most area and timing efficient way.
- Utilization aware placement that meets performance targets while ensuring optimum utilization.

The output is a legal DEF placement optimized to meet your performance and cost objectives. Timing closely correlates with that of the final routed design, so you know that your design will continue to meet timing after Fujitsu routes it.

Exceptional performance, density, and productivity with floorplanning and physical analysis

Amplify AccelArray Pro software provides an easy-to-use floorplan creation and editing environment from which you can synthesize and interactively analyze your design. The tool enables:

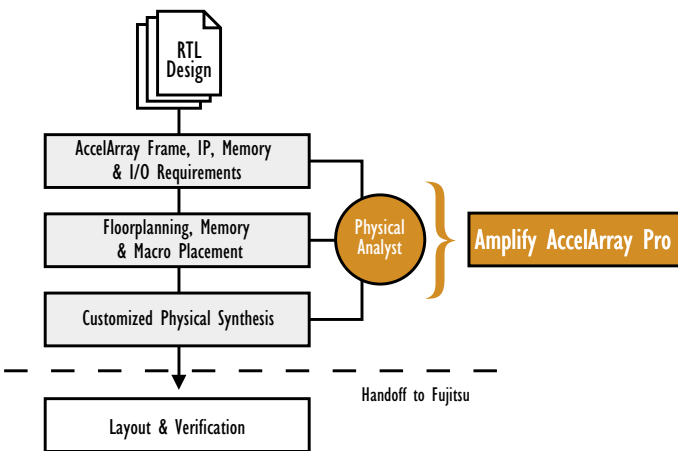
- Floorplan editing.
- Macro and memory placement editing.

Amplify AccelArray Pro Features	Benefits
Recommended by and jointly developed with Fujitsu	Proven and integral part of the AccelBuilder flow for rapid design handoff to Fujitsu.
Custom physical optimizations for AccelArray architecture	Denser, faster designs and faster turnaround times. One-pass handoff of legally placed design to Fujitsu, cutting weeks off your design schedule.
Integrated placement engine	Simultaneous synthesis and legal placement ready for handoff to the vendor; no wire load models used and design abides by AccelArray design rules.
Patented SNAP™ technology	Removes routing ambiguities to ensure tight correlation with final routed design (single-pass handoff to vendor) and to prevent crosstalk.
Physical Analyst interactive debug and display environment	Rapid design debugging, tracing, and cross-probing between placement and gate-level views to RTL source code and timing reports. Congestion/row utilization map helps you identify and fix congestion hot spots.
Industry standard interfaces (DEF, LEF, SDC, .lib, VHDL, Verilog) and TCL batch scripting	Re-use existing RTL and constraints from prior designs. Easily automate design flow.
Automatic and manual floorplanning (user can mix-and-match)	Automatic creation and assembly of legal floorplans. Re-use/import existing floorplans and pre-defined macros. Optionally edit the floorplan or set physical constraints to help guide better QoR.
Ultra-fast static timing analysis	Rapid feedback on full chip timing after synthesis and placement.

- Block-based design flows and team-based design — each designer can focus on their portion of the design and work in parallel by designating non-overlapping, top-level bounding boxes or soft regions within the floorplan.
- Interactive physical analysis using the Physical Analyst feature.

Using the Amplify AccelArray Pro floorplanning and physical analysis environment, you can opt to make additional improvements to the timing and density of your design by:

- Setting physical constraints — leading to improved QoR.
- Interactively editing the floorplan.
- Identifying and fixing congestion hot spots prior to routing using the row/utilization map.



Save time with single-pass handoff to Fujitsu

When you use the Amplify AccelArray Pro solution, you save time by performing a single-pass handoff of your design to Fujitsu. The Amplify AccelArray Pro solution is the only physical synthesis tool capable of creating a placed gates design for which:

- **Timing tightly correlates with final routed design, at the time of handoff** — this avoids expensive design iterations between you and Fujitsu.
- **Placement is legal** — the placement abides by AccelArray design rules. Signal integrity/cross-talk issues are prevented.

“Our partnership with Synplicity means that AccelArray customers will see the highest silicon performance, and the rapid turnaround times that they have come to expect from structured ASICs. Fujitsu is pleased to recommend the Amplify AccelArray Pro physical synthesis and floorplanning solution to our AccelArray Structured ASIC customers.”

— Mitsugu Naito
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