

Update Highlights

There will definitely be some atmosphere at the **Actel Space Forum** in The Netherlands on the 31st - **Aldec** will be there in support and to present their **RTAX** prototyping solutions. **Thales** talk about their experience with Aldec's **DO-254 CTS** flow and **Riviera-PRO 2009.02** is released with a host of new features and improvements. Plus you can catch up on the latest webinars from **Aldec**...

Lonsdale's Lounge...

"If ever there was a need for Engineers to ply their trade within strict limits of resources and time, it is now!"



"Working within tight parameters is, of course, the essence of what we do but there is a real danger in the current climate that matters get out of hand and opportunities for working smarter are missed. One trend that is highly evident (and most welcome) is the desire to not over-spend on methodology staples, such as verification. Courtesy of Aldec, you can add features and save money with Riviera-PRO—a fact that many of our new customers can testify to! It's great that we can give you a real choice when it comes to renewal time—we're standing by to take your call!"

Julian

Actel Space Forum

The 2nd European Actel Space Forum will take place in Noordwijk, The Netherlands, on 31 March 2009. Actel's technical specialists and executives will present topics relevant to the use of Actel FPGA's in space applications. Topics will include:



- FPGA devices, development tools and IP roadmaps for space
- Design techniques to optimise power consumption, improve timing performance and make best use of available device resources
- Radiation, qualification and reliability update

Aldec and FirstEDA will also be there to present how our RTAX adaptor prototyping technology can achieve substantial savings.

[Click here to read about Aldec's RTAX solution...](#)

[Click here to download our recent Aldec RTAX webinar...](#)

[Click here to register your interest directly with Actel...](#)

To be Sure...to be Sure...to be Sure!



Verification is the most important part of the FPGA / ASIC design process and Aldec make it their business to lead in this arena with a range of products to suit.

To cement their leadership and expertise in the verification space, Aldec continue to produce successful webinars, often in conjunction with specialist partners. The aim, to deliver hot topics and relevant content direct to your desktop!

Recent webinars include:

- Migrating to Transaction-level Modelling in SystemC
- Start using Assertions in your next design
- SystemVerilog Assertions—Methodology and Language Overview
- Design Rule Checking Tools: a key to avoiding ASIC Re-spins

[Click here to see the Aldec webinar archive...](#)

VHDL Lint—A STARC Reality...



Following the successful introduction of Verilog STARC rules for ALINT, Aldec will shortly release ALINT 2009.02 with a comprehensive set of VHDL STARC design rules.

STARC stands for Semiconductor Technology Academic Research Center and is a consortium of 11 Japanese ASIC foundries that has established a set of design rule guidelines for corporations to follow based on a set of best-design practices.

Aldec ALINT key features include:

- Fast design analysis of complex ASIC/FPGA-SOC designs
- Comprehensive set of rules to check most complex design issues
- Customisable violation viewer with cross-probing to source code
- Advanced framework to set-up and configure checks
- User modified rules/rule-sets/policies
- Supports VHDL, Verilog and mixed-language designs

[Click here for further information about Aldec ALINT...](#)

Riviera-PRO 2009.02 Released!



Riviera-PRO 2009.02 has just been released and continues to garner acclaim with it's new GUI which runs independently of the simulation kernel to leverage multi-processors platforms.

Other features & improvements for 2009.02 include:

- Significant performance enhancements for both VHDL and Verilog simulations
- A number of important additions to SystemVerilog support
- Enhancements to the assertion evaluation model
- A generic framework provides support for macro conversion from other simulators
- VHDL and Verilog files can now be encrypted with the AES256-CBC cipher
- Further enhancements to the waveform viewer
- MATLAB and Simulink interface now supported on Linux

[Click here to upgrade or evaluate Riviera-Pro 2009.02...](#)

Thales Validates with CTS

Find out how Thales successfully deployed Aldec's DO-254 CTS flow and were able to uncover & resolve design issues not visible in simulation...



Out of Date?

Aldec	
Active-HDL	8.1-SP2
Riviera-PRO	2009.02
ALINT	2008.10
Concept	
GateVision PRO	4.4.1
SpiceVision PRO	4.4.1
RTLvision PRO	4.4.1
SGvision PRO	4.4.1
LogicVision	
Dragonfly	7.0
Pinebush	
HyperPlot	6.0