

## Update Highlights

We discuss **UVM 1.1** and how kits can be used to provide interoperability for legacy verification code. Aldec unveils plans for customer based tool webinars. **Active-HDL 9.1** is released with many enhancements including a new code browser and **Riviera-PRO 2011.10** has also just been released with a strong UVM message...

### Lonsdale's Lounge

"An interesting fact, that runs counter to perception from the mass media, is that Xmas parties are back in vogue (bookings are up 300% at hotels in the Bracknell area!) With all businesses watching their bottom line, overworked employees are being rewarded and no doubt reminded that the foreseeable remains just as challenging."



"In our sphere, verification continues to dominate and the good news is that FPGA designers now have access to methodologies that can make a real difference to both quality and productivity. We look forward to continuing to spread the message."

"To all our customers; seasons greetings and best wishes for the new year ahead."

*Julian*

### Complete Support for UVM 1.1



There are two major open source verification methodologies today; Universal Verification Methodology / Open Verification Methodology (UVM/OVM) and Verification Methodology Manual (VMM). Both are complete standalone solutions that approach the structure of verification environments in different ways.

After just a few years of application, a significant amount of legacy code already exists which creates a conundrum when looking to migrate to an alternative library or integrating verification code from one methodology to the other. Well fear not! The latest version of Riviera-PRO brings complete support for the Universal Verification Methodology (UVM) and related extensions comprising the following:

**OVM/VMM Interoperability Kit**, enabling OVM- and VMM-based IP to work together in a single verification environment. The kit contains OVM/VMM interoperability library – a collection of adapters and utilities that enables efficient reuse without the need to modify the legacy code.

**UVM Register Kit**, enabling an easy migration path from OVM to UVM-based verification environments. The kit contains a part of the Accellera UVM reference library – a standard vendor independent register solution that enables migration to UVM without changing the use model.

UVM 1.1 is immediately available with the Riviera-PRO 2011.10 installation.

Click [here](#) for an overview of the Riviera-PRO 2011.10 release.

### What's Your Best Feature?



Do you find yourself upgrading and sticking to a way of working with the tool, uncomfortable with exploring the new features?

Ever think "I wonder if I can do that...?" or "Wouldn't it be good if...?" but you're too busy to ask the question or think it won't be possible...sound familiar?

Based on many such recent customer conversations, Aldec will be putting together some Webinars, targeting our existing users, to showcase not only new features but some methodology tips and other ways to crack nuts. Please look out for our e-mails in the new year.

### Active-HDL 9.1 Released!



Aldec have recently released Active-HDL 9.1 with the following improvement highlights:

- Language enhancements to both VHDL-2008 and SystemVerilog (for design)
- Code Browser allowing design structure to be viewed pre-elaboration. Also does syntax checking 'on the fly'
- Exclude objects from compilation / synthesis in the Block Diagram Editor
- Block diagram now synchronised with waveform allowing 'single click' signal addition from BDE
- Interface to ALINT & Riviera-PRO allowing 'single click' analysis

Click [here](#) to view the release notes.

Click [here](#) for an overview presentation on the 9.1 release.

Already a licensed customer? Then please login to the Aldec [support](#) area to upgrade.

To evaluate Active-HDL 9.1, please go to the [download](#) area where you will be asked to register.

### Riviera-PRO 2011.10 Released!



Aldec have recently released Riviera-PRO 2011.10 with the following improvement highlights:

- The UVM library version 1.1 is now included in the default installation
- SystemVerilog and SystemVerilog Assertion improvements including array manipulation methods and dynamic arrays randomisation
- SystemC—HDL connection—propagate signals from SystemC functions to HDL
- Many new productivity features added

Click [here](#) to view the release notes.

Click [here](#) for an overview presentation on the 2011.10 release.

Already a licensed customer? Then please login to the Aldec [support](#) area to upgrade.

To evaluate Riviera-PRO 2011.10, please go to the [download](#) area where you will be asked to register.

### Sign up for FirstEDA News!

Get the latest news about software releases, service packs, tutorials, tips & tricks and more...



Click the RSS icon for sign up details...

### Out of Date?

|              |         |
|--------------|---------|
| <b>Aldec</b> |         |
| Active-HDL   | 9.1     |
| Riviera-PRO  | 2011.10 |
| ALINT        | 2010.10 |

|                            |       |
|----------------------------|-------|
| <b>Concept Engineering</b> |       |
| GateVision PRO             | 5.3.5 |
| SpiceVision PRO            | 5.3.5 |
| RTLvision PRO              | 5.3.5 |
| SGvision PRO               | 5.3.5 |

|                 |     |
|-----------------|-----|
| <b>Pinebush</b> |     |
| HyperPlot       | 6.0 |