

End-to-End DO-254 Functional Verification

MIL/AERO



DO-254/CTS™

DO-254/CTS is an end-to-end functional verification solution, including: Software, Hardware, Analysis, Documentation and EDA Tool Qualification, for 100% Functional Verification coverage. DO-254/CTS supports the "Design Assurance Guidance for Airborne Electronic Hardware" (DO-254/ED80) chapter 6.2 "Verification Process" assurance levels A, B, C and D; and chapter 11.4 "Tool Assessment and Qualification Process". DO-254/CTS is a patented solution (US Patent 5,479,355).

Top Features

- At-Speed Design Verification in Target Devices
- For use with Actel™, Altera®, Lattice® and Xilinx® devices
- Automatic Test Vector Generation for Target Devices
- Auto-Capture and Analysis of results at all Design Stages
- Easy Design Requirements Traceability
- Independent EDA Tool Assessment
- Significantly shortens Device Verification Time

DO-254/CTS Overview

Responding to design and testbench files, the **Software Simulation** performs RTL, gate and timing-level simulations, shown in Figure 1. This block generates test vectors for driving operation of hardware verification and gold vectors for comparison with corresponding hardware outputs. Code Coverage and Design Rule Checking enhance the design and testing quality.

Included Software

- Aldec HDL Simulator (optional)
- Aldec Waveform Viewer and Code Coverage
- Design Rule Checking

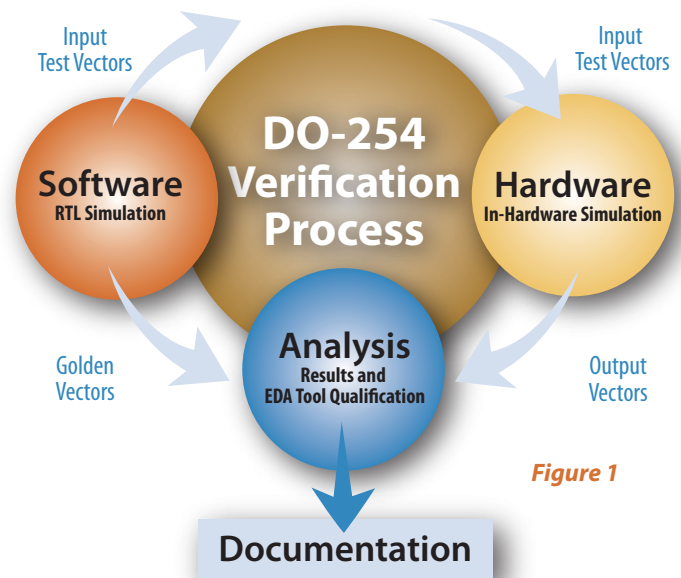


Figure 1

The **In-Hardware Simulation** block facilitates at-speed design verification. Its output vectors are used by the **Analysis** block for comparison with golden vectors produced by software simulations. By comparing results from various simulation levels, this block also validates the synthesis and place-and-route tools.

Included Hardware

- PCI/PCIe Mother Board (MB)
- Custom Daughter Board (DB) with target device
- CVT™ Application (TVD, VT, drivers, API, diagnostic designs)

The **Documentation** block helps to produce documentation required by DER and the DO-254 certification process, including justification for the assessment decisions, tool qualification data, and documentation required by the chapter 11.4 of the DO-254 specification.

Methodology Diagram

Aldec DO-254/CTS methodology consists of four levels of verification as seen in Figure 2 below. The first three blocks (1, 2 and 3 *Software*) verify the design behavior at the RTL, gate and timing levels. The verified data can then be used for independent tool assessment of In-Hardware verification, block (4 *Hardware*).

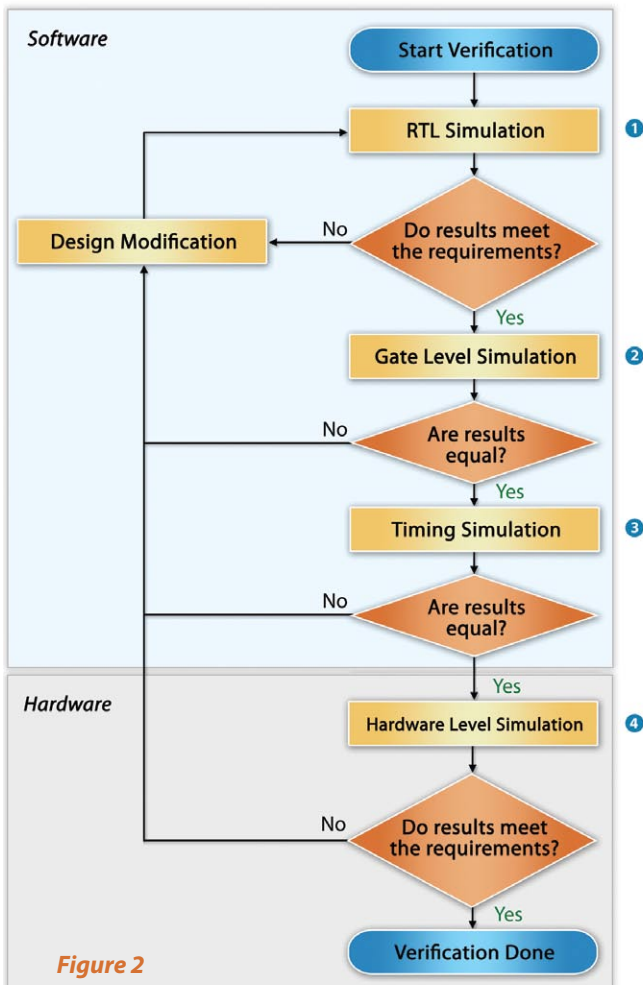


Figure 2

HDL Simulation Tool Suite

Aldec HDL Simulation tool suite supports VHDL, Verilog®, SystemVerilog, Assertions, SystemC/C/C++ and EDIF. It provides HDL simulation (source level), post-synthesis simulation (gate level) and post place-and-route simulation (timing level), in a single software environment, which includes code linting, code coverage, profiling, automated documentation and waveform comparison tools to enhance verification productivity. The HDL simulator uses the testbench to verify the design functionality and provides coverage metrics to measure how effectively the testbench has exercised the design. The simulation results are stored in a waveform format and are automatically compared to the results from various simulation modes to provide synthesis and place-and-route independent tool assessment.

Functional In-Hardware Verification

The In-Hardware verification requires development of test vectors and the target device (FPGA or PLD) bit-file.

- The TVD subroutine automatically dumps test vectors from the testbench used for HDL simulation.
- The bit-file created for timing simulation is downloaded to the target device on the daughter board.

The In-Hardware testing starts with the Verification Tool (VT) software writing the input vectors to FIFO IN on the PCI mother board, shown in Figure 3. Next, VT drives the input vectors to the target device on the daughter board, which generates responses that are stored in FIFO OUT on the mother board. The VT software saves these outputs in the waveform format and records for comparison with the waveform outputs from HDL simulation. The design functionality is considered proven if the output waveforms of In-Hardware testing match the waveforms generated during the HDL simulation.

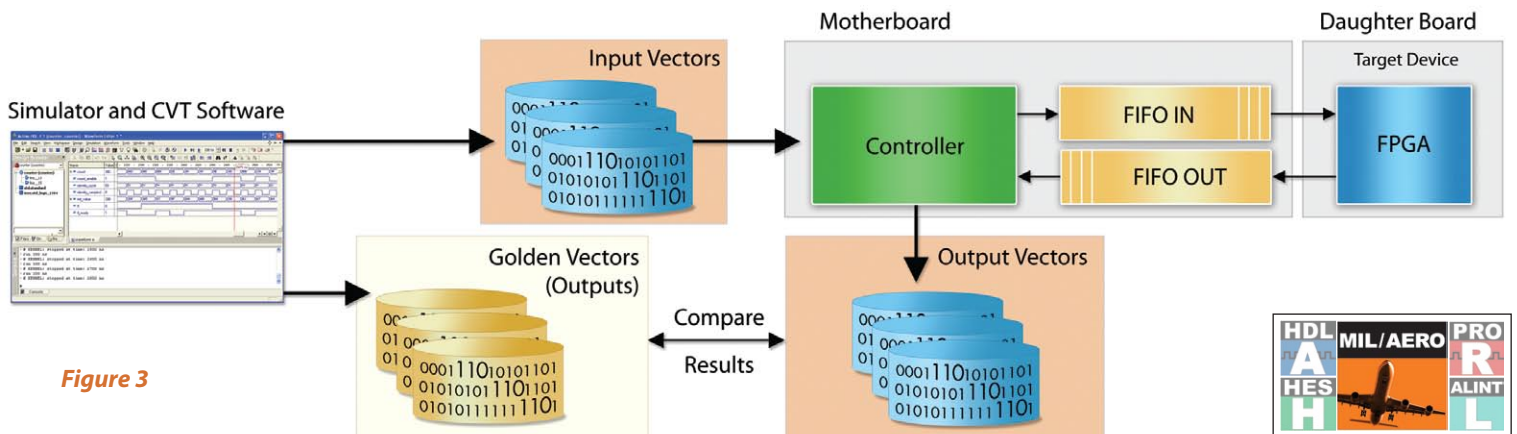


Figure 3



World Wide Web

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