

# Design Rule Checking

 **FIRST EDA**  
enabling design  
FIRST EDA LTD  
Mercia House, South Bar, Banbury, OX16 9AB, UK  
t: +44 (1295) 201250 / f: +44 (1295) 201252  
e: info@firsteda.com / w: www.firsteda.com



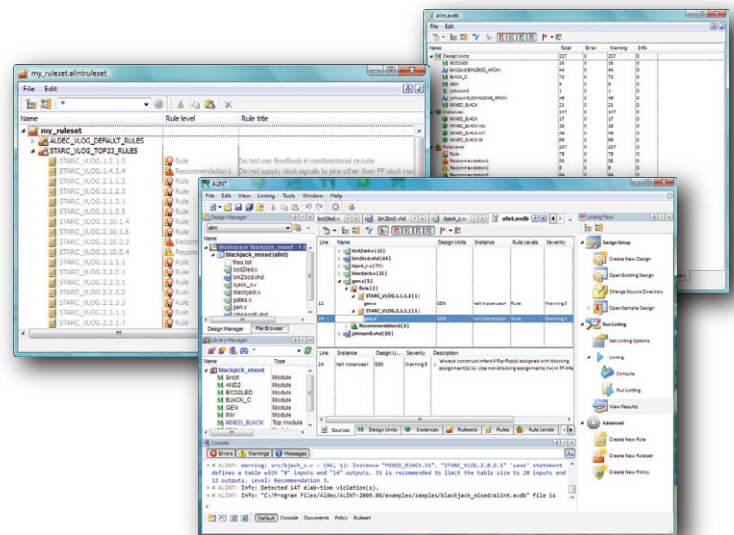
ALINT is an RTL design analysis tool, which identifies potential design issues early in the development cycle. The tool checks VHDL, Verilog® mixed-language designs for structural, coding and consistency issues prior to Simulation and Synthesis. ALINT significantly reduces verification time of complex FPGA and ASIC designs, resulting in uniform, re-usable and reliable code which reduces the risk of costly ASIC re-spins.

## Top Features

- Fast Analysis of complex ASIC/FPGA/SOC designs
- Comprehensive Design Rule Libraries – Aldec, STARC, DO-254 and RMM
- Integrated Results Analysis and Debugging Environment
- IEEE VHDL, Verilog and Mixed-Language support
- User-defined Design Rules (C++ based API)
- Native Support of FPGA Primitives (Altera® and Xilinx®)
- Linux and Windows® 7/Vista/XP/2003 32/64 bit support

## Benefits of Design Rule Checking

Design Rule Checking provides designers with the opportunity to discover complex design issues early in the design flow before Simulation and Synthesis are performed. Design Rule Checking ensures that coding and source code management conventions are followed. It also checks code for synthesizability, to prevent potential simulation problems and eliminate differences between the results of RTL and post-synthesis simulation.



## Prepackaged Design Rules

ALINT offers a set of prepackaged rules that help designers maximize performance of tools for Simulation and Synthesis. The current set of design rules consists of STARC® VHDL, STARC Verilog, RMM (mixed language), Aldec DO-254 and Aldec VHDL/Verilog design rules. The areas covered by the rules include but not limited to: basic design constraints, synthesizable description, reusability, synchronous design, clocks and resets, combinational logic, CDC and DFT.

## Debugging and Results Analysis

ALINT features an Integrated Debugging Environment that includes an HDL Editor and Violation Viewer, which facilitates extensive results analysis and debugging. The Violation Viewer includes an advanced violations summary, cross-probing between violations reports and HDL code, filtering of violations, search, export of linting results and comparison of violation reports from two subsequent linting sessions.



## STANDARDS



## PARTNERS



## FEATURES

General	ALINT
Design Setup/Management	•
Integrated Debugging Environment	•
FPGA Primitive Support (Altera and Xilinx)	•
GUI Mode Execution	•
Batch Mode Execution	•
Supported Languages	
Verilog® IEEE 1364 (1995, 2001 and 2005)	•
VHDL IEEE 1076 (1987, 1993, 2002 and 2008)	•
Configuration and Setup	
Linting Flow	•
User-Defined Rules	•
Configuration Viewer	•
Rule Description Viewer	•
Rule Plug-in Viewer	•
Ruleset Editor	•
Rule Parameters Editor	•
Policy Editor	•
Results Analysis	
Violation Viewer	•
Cross-Probing to Source Code	•
Violation Reports Comparison	•
Design Rule Libraries	
Aldec Basic (VHDL and Verilog)	•
STARC® (VHDL or Verilog)	Option
DO-254 (VHDL or Verilog)	Option
RMM (VHDL and Verilog)	Option
Supported Platforms	
Windows® 7/Vista/XP/2003 32/64 bit	•
Linux 32/64 bit	•

## PRODUCT CONFIGURATIONS

## Prepackaged Design Rules

### STARC® Design Rules

STARC is a consortium of 11 Japanese ASIC foundries that has established a set of design guidelines based on proven, best-design practices. The STARC RTL Design Style Guide for VHDL and Verilog, Second Edition, is used as ALINT's foundation.

### Aldec Design Rules

Aldec offers a mixture of VHDL and Verilog rules. This basic rule set is a starting point for any organization to get started with the tool.

### DO-254 Design Rules

This plug-in provides a set of rules that can be used to improve design compliance with DO-254 requirements. The main topics covered by the rules are: good coding practices, design reviews, safe synthesis.

### RMM Design Rules

Reuse Methodology Manual (RMM) design rule library is based on the industry-proven manual from Synopsys Inc. and Mentor Graphics Corp. which defines the methodology for effective design reuse and verification.

## Create Custom Rules

ALINT's programming interface can be used by designers to implement their own rules as well as company-specific guidelines. An embedded C/C++ API wizard simplifies the process of creating new rules. All necessary templates are created automatically and should be completed by designers for the desired functionality. Once created, the user-defined rules are managed by the tool in the same way as prepackaged rules.

## Design Management

ALINT provides a customizable framework that includes a set of powerful utilities for design management, result analysis and debugging. A Design Manager allows viewing and management of designs and their resources. The Rule Plug-in Viewer provides fast access to prepackaged rules. A Violation Viewer allows detailed and efficient analysis of results.



### Headquarters

2260 Corporate Circle  
Henderson, NV 89074  
Phone: 702.990.4400  
Fax: 702.990.4414  
E-mail: sales@aldec.com

### Europe

70 rue Cortambert  
75116 Paris, France  
Phone: 33.6.80.32.60.56  
Fax: 33.1.46.34.85.91  
Email: sales-eu@aldec.com

### Japan

Shinjyuku Estate Bldg. 9F  
1-34-15, Shinjyuku, Shinjyuku-ku  
Tokyo 160-0022, Japan  
Phone: 81.3.5312.1791  
Fax: 81.3.5312.1795  
Email: info@aldec.co.jp

### China

Suite 2004, BaoAn Building  
#800 DongFang Road  
PuDong District  
Shanghai City 200122, P.R. China  
Phone: 86.21.6875.20.30  
Fax: 86.21.6875.0083  
Email: info@aldec.com.cn

### India

P-186, Sector 10  
Jiwan Bima Nagar  
Bangalore  
India-560075  
Phone: 91.80.4150.6434  
Email: sales-sa@aldec.com

