

# Fast RTL Simulation Engine



**FIRST EDA LTD**  
Mercia House, South Bar, Banbury, OX16 9AB, UK  
t: +44 (1295) 201250 / f: +44 (1295) 201252  
e: info@firsteda.com / w: www.firsteda.com



## Riviera-PRO™

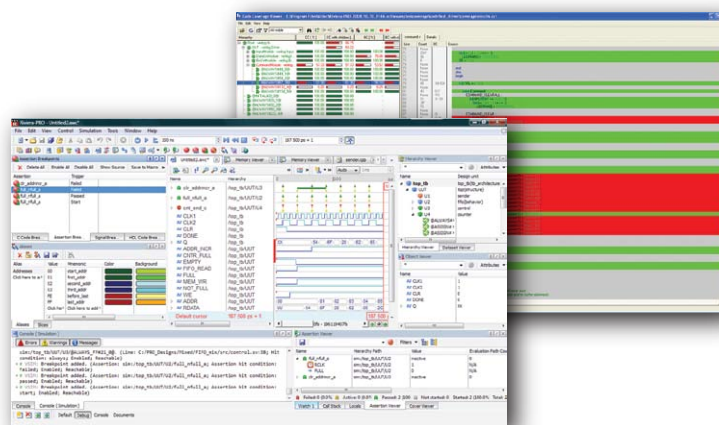
Riviera-PRO is a common-kernel, multi-platform RTL Simulator for mixed-language VHDL, Verilog®, SystemVerilog, SystemC/C/C++ and EDIF designs. Riviera-PRO works in command line mode for maximum speed and includes enhanced editing, tracing, debugging and code coverage. Riviera-PRO supports the most advanced verification methodologies, including: ESL, TLM, OVM, VMM and Assertion-Based Verification (ABV).

### Top Features

- High-performance, common-kernel RTL Simulator
- IEEE VHDL, Verilog®, SystemVerilog, SystemC/C/C++
- Advanced Verification (ESL, TLM, OVM and VMM)
- Assertions and Functional Coverage (SVA, PSL and OVA)
- Ultra-fast Debugging
- Accelerated Waveform Viewer
- Code Coverage
- DSP Co-Simulation with MATLAB® and Simulink®
- Linux and Windows® 7/Vista/XP/2003 32/64 bit support

### High-Performance RTL Simulator

Riviera-PRO includes our highest performance RTL simulation engine for timing, gate-level designs and behavioral code. Riviera-PRO includes simulation performance optimization technology for VHDL and Verilog designs, increasing performance over 6X. The product provides a simulation performance metrics profiler, support for VCD, Open IP encryption and pre-compiled FPGA vendor libraries.



### Advanced Verification

Riviera-PRO supports the most advanced verification methodologies, System Level Design and libraries. Riviera-PRO provides System Level Verification utilizing SystemC with its Transaction Level Models (TLM) and SystemVerilog verification methodologies. The product includes seamless integration of Assertions and Functional Coverage for SystemVerilog, PSL and OVA assertion languages. Riviera-PRO supports SystemVerilog-based Open Verification Methodology (OVM) and Verification Methodology Manual (VMM) libraries.

### World Class Debugging Tools

Riviera-PRO provides ultra-fast graphical debugging tools, including a high-performance Waveform Viewer for quick tracing of signals, their relationships and setting breakpoints. Riviera-PRO gives engineers full access to a post-debugging toolset and SystemC/C/C++ support. A powerful code coverage analyzer helps in achieving 100% test coverage of all RTL code/lines, statements, branches, logical expressions, path and toggle values.



## STANDARDS



## SILICON



## INTERFACES



## FEATURES

	LV	LVT	LVT-SV
<b>Supported Languages</b>			
VHDL IEEE 1076 (1987, 1993, 2002 and 2008)	•	•	•
Verilog® HDL IEEE 1364 (1995, 2001 and 2005)	•	•	•
SystemVerilog IEEE 1800™-2005 (Design)	•	•	•
SystemC™ 2.2 IEEE 1666™/OSCI 2.2/TLM 2.0	•	•	•
SystemVerilog IEEE 1800™-2005 (Assertions)	•	•	•
SystemVerilog IEEE 1800™-2005 (Verification)	•	•	•
<b>Design Entry and Design Management</b>			
HDL Editor with Syntax highlighting and Auto-Complete	•	•	•
File Browser, Design and Library Managers	•	•	•
Customizable GUI Perspectives	•	•	•
Macro, Tcl/Tk, Perl script support	•	•	•
<b>HDL Debug and Analysis</b>			
Interactive Code Execution Tracing	•	•	•
Advanced Breakpoint Management	•	•	•
Accelerated Waveform Viewer (ASDB)	•	•	•
Hierarchical References to/from VHDL (Signal Agent)	•	•	•
Post-Simulation Debug	•	•	•
Waveform Compare	•	•	•
Assertions in Waveform and Debugging	•	•	•
Memory Viewer	•	•	•
Integrated C/SystemC Debugger	•	•	•
X-Trace	•	•	•
Advanced Dataflow	•	•	•
<b>Simulation/Verification</b>			
Single or Mixed Language	•	•	•
Verilog Programming Language Interfaces (PLI/VPI)	•	•	•
VHDL Programming Language Interface (VHPI)	•	•	•
SystemVerilog IEEE 1800™-2005 DPI 2.0	•	•	•
Value Change Dump (VCD and Extended VCD) Support	•	•	•
Incremental Compilation	•	•	•
Multi-Threaded Compilation	•	•	•
32/64-Bit Cross-Compatible Libraries	•	•	•
Simulation Model Protection/Library Encryption	•	•	•
VHDL 2008 and Verilog 2005 IEEE Encryption	•	•	•
Xilinx® SecureIP Support	Option	•	•
Verilog and VHDL Performance Optimization	•	•	•
64-bit Simulation	•	Linux Only	Linux Only
Profiler (Performance Metrics)	•	•	•
SFM (Server Farm Manager)	•	Option	•
HES™ Hardware Assisted Verification (Acceleration and Emulation)	•	Option	Option
<b>External Simulation Interfaces</b>			
Synopsys® SmartModels, SWIFT Interface and LMTV	•	•	•
SpringSoft® Verdi™ PSD mode Interface	•	•	•
<b>Coverage Tools</b>			
Code, Statement, Branch, Expression, Condition, Path and Toggle Coverage	•	•	•
Functional Coverage in Assertions/Code Coverage	•	•	•
Aldec Coverage Database (ACDB) – SystemVerilog Functional Coverage Only	•	•	•
Coverage Viewer with HTML/TXT Reporting	•	•	•
Path Coverage (VHDL Only)	•	•	•
<b>Co-simulation</b>			
Simulink® Co-simulation	•	•	•
MATLAB® Co-simulation	•	•	•
<b>Assertions Bundle</b>			
PSL IEEE 1850, SystemVerilog IEEE 1800™, OpenVera Assertions	•	•	•
<b>Design Rule Checking</b>			
ALINT™ with Aldec Basic Rule Library	Option	•	•
DO-254 VHDL or Verilog Rule Library	Option	Option	Option
STARC® VHDL or Verilog Rule Library	Option	Option	Option
RMM Rule Library	Option	Option	Option
<b>Supported Platforms</b>			
Windows® 7/Vista/XP/2003 32/64 bit	•	•	•
Linux 32/64 bit	•	•	•

## PRODUCT CONFIGURATIONS

**Headquarters**  
2260 Corporate Circle  
Henderson, NV 89074  
Phone: 702.990.4400  
Fax: 702.990.4414  
E-mail: sales@aldec.com

**Europe**  
70 rue Cortambert  
75116 Paris, France  
Phone: 33.6.80.32.60.56  
Fax: 33.1.46.34.85.91  
E-mail: sales-eu@aldec.com

**Japan**  
Shinjyuku Estate Bldg. 9F  
1-34-15, Shinjyuku, Shinjyuku-ku  
Tokyo 160-0022, Japan  
Phone: 81.3.5312.1791  
Fax: 81.3.5312.1795  
E-mail: info@aldec.co.jp

**China**  
Suite 2004, BaoAn Building  
#800 DongFang Road  
PuDong District  
Shanghai City 200122, P.R. China  
Phone: 86.21.6875.20.30  
Fax: 86.21.6875.0083  
E-mail: info@aldec.com.cn

**India**  
P-186, Sector 10  
Jiwan Bima Nagar  
Bangalore  
India-560075  
Phone: 91.80.4150.6434  
E-mail: sales-sa@aldec.com



www.aldec.com