

Corporate Fact Sheet



Company Overview

Aldec, Inc. is an industry-leading Electronic Design Automation (EDA) company delivering innovative design creation, simulation and verification solutions to assist in the development of complex FPGA, ASIC, SoC and embedded system designs.

With an active user community of over 35,000, 50+ global partners, offices worldwide and a global sales distribution network in over 43 countries, the company has established itself as a proven leader within the verification design community.

Founded

1984 by Dr. Stanley M. Hyduke

Holdings

Privately held, revenue-funded

Employees

Approximately 200 worldwide

Corporate Headquarters

2260 Corporate Circle,
Henderson, NV 89074
Phone: 702.990.4400

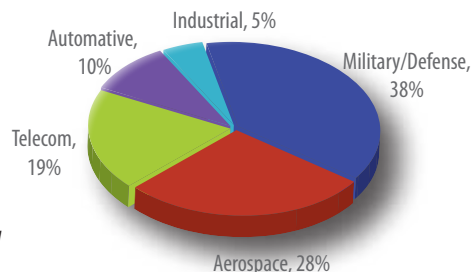
Office Locations

China	Japan	UK
India	Poland	Ukraine
Israel	Taiwan	USA

Market

Aldec market share is estimated at 38% of all mixed-language RTL Simulators sold to FPGA designers worldwide.

Excludes OEM simulators supplied directly from FPGA vendors.



Aldec delivers high quality EDA solutions for government, military, aerospace, telecommunications, automotive and safety critical applications. Large companies such as IBM, GE, Qualcomm, Rohde and Schwarz, Bosch, Texas Instruments, Applied Micro, Hewlett Packard, Toshiba, Intel, NEC, Mitsubishi, LG, Hitachi, NASA, Invensys, Westinghouse, Raytheon, Panasonic, Lockheed Martin, Samsung, as well as mid-size to small firms utilize Aldec EDA verification suites to boost product performance, cut design development cycles and reduce costs.

Proven Solutions

From the development of small IC designs to large, 100 million gate ASIC's—a proven EDA solutions provider makes all the difference to a successful and accurate verification deployment. Aldec understands the high importance design teams place on quality, productivity and increasing time-to-market pressure. The company shares these values in its commitment to supplying robust solutions that support the latest Design Creation and Verification methodologies. Our promise to deliver leading verification methodologies that support the latest IEEE and Accellera language standards allows our customers to grow while leveraging evolving technologies.

DESIGN CREATION

Even simple designs contain multiple files that must be modified frequently and processed by multiple tools (simulators, synthesizers, and implementation engines). Aldec provides solutions that allow entry and management of sources textually and graphically, working with VHDL, Verilog, SystemC, SystemVerilog and many other formats.



VERIFICATION

The size and complexity of modern designs makes it necessary to verify their behavior before silicon is manufactured. Aldec offers powerful design rule checkers, simulators and co-simulation solutions that can be helpful in any design environment.



SPECIALTY SOLUTIONS

Aldec provides solutions that serve Military/Aerospace, Safety-Critical, and Microsemi™ RTAX Prototyping.

DO-254 CTS
Certifiable Testing Environment
for Level A/B Designs

RTAX Prototyping
Hardware Adaptor
RTAX-S/SL, AX, RTSX-SU/SX-A

Our Partners

UNITE PARTNERS

achronix Agnisys ALTERA Altium ARM
 AVNET berkeley design automation, inc. bluespec cadence The Dini Group
 EMA Design Automation Lattice Semiconductor Corporation MAGMA Mentor Graphics
 Microsemi QuickLogic SpringSoft SYNOPSIS
 tabula The MathWorks XILINX ZUKEN

IP PARTNERS

CAST HELIX NORTHWEST LOGIC
 pld applications stream DSP

TRAINING PARTNERS

CBE SynchWorks
 DOULOS

STANDARDS ORGANIZATIONS

accellera EDA CONSORTIUM IEEE QVM
 SYSTEMC SystemVerilog UVM

Key Milestones

2011

- Opens Office in the UK Supporting Europe
- Avnet Asia Pacific Distributes Aldec FPGA Simulator
- UVM 1.0, OVM 2.1.2 & VMM 1.1.1a Support
- Mirror-Box™ Debugging Technology
- Releases 4 MHz Design Emulator
- Best FPGA Design & Verification Platform Provider, China

2010

- Opens Offices in Taiwan and Israel
- Active-HDL: Best FPGA Design & Simulation Tool in China
- Altium Embeds Aldec Simulator in Altium Designer
- Releases Support for VHDL IEEE 1076-2008

2009

- Opens Office in India
- Releases DO-254 Design Rule Library for ALINT
- Avnet Japan Distributes Aldec FPGA Simulator

2008

- Releases ALINT™: Design Rule Checker (STARC – Japanese Consortium of 11 ASIC Companies)

2007

- Opens Office in Japan
- Releases DO254-CTS (Compliance Tool Set)
- Releases Actel (Microsemi) Prototyping Solution – RTAX-S Antifuse to Flash Device
- Signs OEM agreement with Lattice® Semiconductor

2006

- Opens Offices in Beijing and Shanghai, China
- Aldec Is Ranked No. 3 in FPGA User Survey
- Aldec Is Awarded Patent for ClockConversion™

2005

- Releases Optimized Verilog Simulator, Based on Support for 32 and 64-bit Simulation Technology

2004

- Releases SystemVerilog & SystemC Design Tools

2003

- Releases HES™: Hardware Emulation, Acceleration & Prototyping Solutions

2002

- Releases Riviera-PRO™: Multi-Platform Software Simulator
- Aldec Named Southern Nevada Distinguished Business of the Year, Nevada Economic Commission

2000

- Signs Strategic OEM Agreement with Synplicity®

1999

- Signs Strategic OEM Agreement with Cypress®

1997

- Releases Active-HDL™: Graphical Design Entry & Mixed Language Simulator

1996

- Signs Strategic OEM Agreement with Xilinx®

1992

- Releases Active-CAD™: a Windows Based Schematic & Gate Level Simulator

1985

- Releases SUSIE™ (Standard Universal Simulator for Improved Engineering), DOS Simulator

1984

- Company Is Established

Technology Patents

- **US Patent #4,791,357:** Electronic circuit board testing system and method
- **US Patent #4,827,427:** Instantaneous incremental compiler for producing logic circuit
- **US Patent #5,479,355:** System and method for closed loop operation of schematic designs with electrical hardware
- **US Patent #5,051,938:** Simulation of selected logic circuit designs
- **US Patent #6,578,133:** MIMD Array of Single Bit Processors for Processing Logic Equations in Strict Sequential Order
- **US Patent #6,915,410:** Compiler synchronized multi-processor programmable logic device with direct transfer of computation results among processors
- **US Patent #7,003,746:** Method and apparatus for accelerating the verification of application specific integrated circuit designs

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