

Product Line



Design Creation

HDL Active-HDL™: FPGA Design and Simulation

High-performance, mixed-language simulator with design creation, documentation, code coverage and simulation bundled into one product. Active-HDL features an easy-to-use, FPGA flow manager that controls VHDL, Verilog, SystemVerilog and SystemC simulation, synthesis and implementation for Altera®, Lattice®, Microsemi™ and Xilinx®. Each operation is invoked from a central location and all files are managed from one common environment independent of FPGA vendor.

Advanced Debugging

Verification

PRO Riviera-PRO™: Verification Platform

Riviera-PRO is based on IEEE and Accellera language standards and delivers a mixed language verification platform focused on performance quality and support of industry standards. The UVM and VMM verification methodologies enable users to leverage verification libraries to build layered coverage-driven and transaction-level verification environments. Integrated multi-core compiler and advanced graphical and script based debugging environment extend the usage of the powerful simulator by providing intuitive ways to visualize and analyze key design objects.

ALINT ALINT™: Design Rule Checking Tool

Checks RTL code for coding style, functional, and structural problems in Verilog, SystemVerilog, VHDL and mixed-language designs to assist in preventing design issues from spreading into the downstream stages of your ASIC and FPGA designs. Sophisticated static analysis techniques uncover a variety of hidden bugs at the right time when cost and efficiency of modifications are optimal and reduce the risks of redundant design iterations and costly re-spins.

Emulation

HES Hardware Emulation Solution

HES™ is a complete ASIC/SoC hardware-assisted verification solution that provides a unified platform for bit level simulation acceleration, transaction level emulation, HW/SW co-verification, virtual modeling and prototyping. HES is equipped with state-of-the-art emulation setup software facilitating easy design setup, ASIC to FPGA clock conversion, automatic design partitioning, advance HDL compiler and extensive debugging capabilities.

Specialty Solutions

MIL/AERO Microsemi® Prototyping: RTAX-S/SL

The Aldec prototyping adaptor board maps the footprint of the Microsemi (Actel) ProASIC3E FPGA device to the footprint of the Actel RTAX-S/SL, RTAX-DSP or RTSX-SU devices for functional verification. After soldering the adaptor to the PCB, a programming connector (JTAG) provides on-the-fly reprogramming device, without detaching the adaptor from the PCB. In addition, a GUI-based EDIF Netlist Converter Application, is available for automatic pin re-mapping from anti-fuse to flash-based architecture.

Quality & Compliance

MIL/AERO DO-254 Compliance Tool Set

Certifiable at-speed in-target testing of programmable logic is a fundamental requirement to achieve level A or B compliance. The DO-254 CTS solution is dedicated to address the stringent guidelines of DO-254 Chapter 6.2 Verification Process. The CTS includes a fully customized hardware and software package design that replays RTL simulation during target hardware testing without any changes to the DUT and testbench. It provides a single and automated environment to test all FPGA level requirements ideal for DO-254 hardware verification, complete with tool assessment packages to validate code coverage results.



Customer Stories

Active-HDL™



"With a good editor/compiler and a versatile, easy to use simulator, Active-HDL was considered the best featured design tool compared to leading competitors. The quality of the design environment and good integration with source control tools definitely saves time on both new development and maintaining existing code."

Riviera-PRO™



"Riviera-PRO provided Infinita with high speed simulation of high-density Verilog design with DPI connections for system software integration. Riviera-PRO is used by individual engineers for interactive debugging and regressions on an automated, multi-node simulator farm."

DO-254/CTS™



"Our project involved an Altera® Cyclone® II FPGA with multiple clocks and speeds in excess of 128 MHz. We wanted a complete verification path with requirements traceability and simulation results maintenance to validate that our system would work on the final hardware we deliver to our customer. Aldec's DO-254/ED-80 CTS gave us an effective way to meet the Level B Verification process requirements imposed by the DO-254 certification authorities."

ALINT™



"Prior to using ALINT from Aldec, all VHDL code had to be personally reviewed by a principal engineer. This was becoming an increasingly laborious task consuming large amounts of valuable time and had the potential to miss errors – especially in larger projects. Using ALINT means that code can be checked by a design engineer much earlier in the design cycle, thus increasing effectiveness and reducing development time by reducing code errors. The final review can now rely on the ALINT reports – simplifying the process, thus reducing the time taken for approval."

Technical Support



"Thanks to Aldec's support team, learning how to simulate a new and rather complex design took nearly no time at all. It is quite clear that Aldec's engineers have left no stone unturned in their quest for excellence."

Microsemi® RTAX Prototyping



"We had a very aggressive schedule. We needed a way to quickly verify the design functionality and integrate support. The Aldec prototyping adaptor saved us two months off our development schedule and over \$72,000 off our project costs."

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