# Intermediate VHDL

## Introduction
Ready for the next step?
For those already familiar with VHDL (either through an introductory course or self-taught), this workshop will broaden knowledge and enforce competency through application.

## Overview
Our three (3) day instructor led workshop is specifically constructed to bridge the gap between basic working knowledge of VHDL and our *Advanced VHDL Verification & Testbenches* course.

As part of our well regarded VHDL training series, our courses are all delivered by time-served engineers in the field of language-based design & verification. Our methodology experts are able to provide insights that go beyond theory, and this ensures practical benefit is gained immediately.

## Objectives
- To provide practical experience in writing, testing and synthesing VHDL code as well as how to implement it on an FPGA
- To enhance your current understanding of VHDL through problematic hardware coding issues
- To introduce you to transaction-based testbenches
- To introduce FSM coding techniques
- To provide VHDL hardware experience with an FPGA lab board

## Duration
Our standard course is based around a three-day agenda. As the material is highly modular, we can also offer customised versions of this course, on-site or at a location of your choice.

## Requirements
Delegates should be familiar with digital design and have a basic understanding of VHDL. Although not essential, an understanding of other HDL or programming languages is an advantage.

## Description
Delivered through a series of lectures, exercises and labs, the training is designed to build upon existing VHDL knowledge acquired through hands-on experience or through introductory VHDL training, such as our *VHDL for FPGA Designers* course.
The training covers both syntax and coding style guidelines in depth, followed by practical exercises designed specifically to reinforce the lecture material. Design projects utilise all techniques learned in the lectures and demonstrate how VHDL is used in a project environment.

## Agenda
RTL Essentials
Data Objects
Testbench Essentials
Subprograms
Testbenches and Timing
VHDL I/O (TEXTIO)
RTL Code
Numeric Types
Design Organisation
Take Home Labs
Digital Clock

## Course Labs
Practical labs account for 50% of the course material and range from simple simulation and synthesis coding problems through to small design projects. Utilising all the techniques imparted in the lectures, the labs provide invaluable hands-on experience of writing RTL code, developing VHDL testbenches, running simulation and programming an FPGA development board.

The labs utilise Aldec Active-HDL, the intuitive class-leading FPGA design and simulation environment.

## Delegate Takeaways
Each delegate is provided with a high quality lecture book and detailed lab book supporting all of the material covered during the course. Each delegate will also be provided with an FPGA development board which is used during the lab exercises and can be used after the course to further expand VHDL knowledge through the takeaway digital clock lab.

For pricing, schedule and to book, please contact us at:

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