FIRSTEDA
ENABLING DESIGN

Advanced VHDL Testbenches & Verification

with **Jim Lewis** of **SynthWorks**

Introduction

Developed and delivered in person by VHDL specialist Jim Lewis, this 5-day instructor led workshop will teach the latest verification methodologies for FPGA and ASIC design. Jim is a founding member of the Open Source VHDL Verification Methodology (OSVVM) and he will instruct you on how to create a VHDL testbench environment that is competitive with other advanced verification methodologies, such as those based on SystemVerilog and 'e'.

Overview

This course will teach you advanced VHDL coding styles, techniques and methodologies. These approaches will ensure that you become more productive at both design verification generally and specifically in regards to testbench development. Your existing investment in VHDL is leveraged and core topics such as data structures, randomisation and coverage are explored in depth.

The course starts with simple testbenches, progressively increasing the level of abstraction and contains numerous examples that can be used as templates to accelerate your own test and testbench development. The final result is a system-level, transaction-based, self-checking test environment.

This methodology uses the natural concurrency that is built into VHDL. Certain processes and models are used to create separate threads of execution for items that naturally run independently. When modelling state machines with this approach they can either be modelled concurrently, like RTL code, or sequentially like software and OO approaches. To synchronise the separate processes, we use a synchronisation primitive from a "library" contained in our open source utility package. Unlike other verification languages, the structure of the testbench is created with structural code similar to RTL, all in VHDL.

Objectives

- Improve design verification and testbench productivity
- Learn how to create a transaction-based, system-level, self-checking test environment
- Implement interface functionality with either a sub-program or bus functional model (aka transaction-level model or TLM)
- Use sub-programs to abstract interface actions (CpuRead, CpuWrite, UartSend)
- Write directed, algorithmic, constrained random, coverage driven random tests or a mixture of them
- Write a test plan that maximises reuse from RTL to core to system-level tests
- Reuse SynthWorks' packages for constrained random testing, functional coverage, memories, scoreboards and interfaces
- Model interface behaviour with proper timing
- Model analogue values and periodic waveforms
- Use VHDL's file read and write capabilities effectively

Requirements

Suitable for device (PLD/FPGA/ASIC) designers who are looking to improve their verification efficiency and effectiveness. Delegates should have a good working knowledge of digital circuits and prior exposure to VHDL through work or a previous course.

Agenda

Day 1, Module TB1
Testbench Overview
Basic Testbenches
Transactions & Sub-programs
Modelling for Verification
VHDL IO

Day 2, Module TB2
Lab Review: Testing with sub-programs
Transaction-based Models (BFM)
Elements of a Transaction-based BFM Part 1
Data Structures for Verification

Day 3, Module TB3
Lab Review: UartTx BFM
Creating Tests
Constrained Random Testing
Functional Coverage

Day 4, Module TB4
Execution & Timing
Configurations & Simulation Management
Advanced Coverage
Advanced Randomisation

Day 5, Module TB5
Lab Review: Scoreboards, Randomisation & Coverage
Modelling RAM
Test Plans
Transaction-based BFM Part 2

Approach & Labs

This hands-on, how-to course is taught by an experienced verification engineer with specialist VHDL knowledge and expertise. We believe that student and instructor interaction is key to a successful learning environment, therefore places on the course are limited.

The course is split roughly 50/50 lecture and labs, so plenty of opportunity to reinforce the theory. Each delegate will be provided with access to a laptop, Aldec Riviera-PRO and all the necessary resources required.

CONTACT

www.firsteda.com
FirstEDA +44 (1295) 201250 or adam.wilson@firsteda.com
Eastlands II, London Road, BASINGSTOKE, RG21 4AW, UK